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L4: Entry 66 of 96 File: USPT Oct 12, 1993

DOCUMENT-IDENTIFIER: US 5253255 A
TITLE: Scan mechanism for monitoring the state of internal signals of a VLSI microprocessor chip

Abstract Text (1):
A VLSI chip debug and production test apparatus that allows an engineer to view the state of hundreds of signals internal to a chip in real-time without probing, which greatly simplifies the isolation of circuit, speed, logic, and microcode bugs. For production testing, it also provides the ability to check the state of these internal signals on a clock-by-clock basis. The mechanism uses a gated XOR-input serial shift-register cell (10), which is stepped out underneath major buses in otherwise unpopulated areas of the chip. Several of these cell groups are linked together to form a scanout path of the desired length, the operation of which is controlled with a single input pin (40). Output data is channeled through a shared output pin (19) to a VLSI tester (16). In the tester (16) the data (19) is checked and accumulated by back-end software over multiple test-loop iterations, and formatted into a readable form.

Detailed Description Text (15):
The scanout mechanism greatly accelerates the silicon debug effort common in early steppings of complex chips. It provides a quick view of the state of hundreds of chip-internal signals without probing, using a lab workstation to view the data. The value of the sampled state is displayed on a per-clock basis, much like a microsimulator's trace or view event format, showing assembler mnemonics, decoded fields, and hexadecimal representation of data. Depending on the speed of the tester, this information can be seen in what appears to be real-time. Circuit failures sensitive to frequency, voltage, or temperature variation can be observed to happen in the lab as these parameters are adjusted. For example, a high-voltage failure can be observed and investigated by increasing the power supply voltage until the scanout display shows a signal mismatch. This mismatching signal or bus indicates which logical block has the failure, and thus the probable bug location is effectively isolated to a group of a few hundred transistors. If further investigation is necessary, conventional silicon debug tools and techniques can be used to rapidly find the exact failure point.

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Terms	Documents
L5 and (on-line or bist)	31

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DATE: Tuesday, December 03, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L7	L5 and (on-line or bist)	31	L7
L6	L5 same (on-line or bist)	3	L6
L5	L3 same test$	404	L5
L4	L3 same clock	96	L4
L3	L2 same l1	2319	L3
L2	real adj1 time	83280	L2
L1	probe or probing	123852	L1

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Search Results -

Terms	Documents
L7 and (probe or probing)	21

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Search: L8

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DB=USPT; PLUR=YES; OP=OR			
L8	L7 and (probe or probing)	21	L8
L7	L6 and l4	41	L7
L6	real adj1 time	83280	L6
L5	L4 same prob$	2	L5
L4	L3 same l2	66	L4
L3	test same debug	1271	L3
L2	on-chip	12397	L2
L1	system adj1 operarating adj1 signal	0	L1

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L7: Entry 15 of 31 File: USPT May 18, 1999

DOCUMENT-IDENTIFIER: US 5905738 A
TITLE: Digital bus monitor integrated circuits

Brief Summary Text (5):
The ability to dynamically (i.e., during normal operation of the circuit board) observe the data passing between integrated circuits in real-time allows monitoring of the functional interactions between multiple integrated circuits on a board. Such a test can reveal timing sensitive and/or intermittent failures that would otherwise not be detectable without the use of expensive testers and mechanical probing fixtures. The ability to dynamically observe system data buses in real-time facilitates system integration, environmental chamber testing, remote diagnostic testing, and built-in self testing.

Detailed Description Text (5):
In operation, the DBMs 20 and 22 are used to observe and test the buses 14-18 connected between the two integrated circuits 10 and 12. DBM devices operate in two modes: off-line test mode and on-line test mode. In the off-line mode, board circuitry is placed in a test mode and control for signal monitoring is input to the DBMs 20 and 22 from the external test bus interface. The external test bus interface includes four signals: TCK, TMS, TDI, and TDO. TCK and TMS are the test clock and test mode select signals, respectively, from the external test controller. TDI and TDO are the serial test data input and output signals used to connect DBM and other devices conforming to the IEEE interface specification. Using the on-line mode, the board circuitry is functioning normally, and control for monitoring comes from the DBMs internal event qualification module (EQM) which is described in detail in connection with FIG. 7.

Detailed Description Text (9):
When the circuit of FIG. 1 is on-line and functioning normally, the first and second DBMs 20 and 22 can continue to monitor the data and address buses 14 and 16 using the internal EQM circuitry described below. During on-line monitoring the internal EQM of each DBM device 20 and 22 outputs control signals to capture the data appearing on the ODI inputs of the respective DBMs. The internal EQM operates synchronous to the control signal outputs from IC1 10 which are input to each DBM via the CK inputs. To know when to capture data, the EQM circuitry within each DBM 20 and 22 has comparator logic which can match the data appearing on the ODI inputs against a predetermined expected data pattern or set of expected data patterns.

Detailed Description Text (45):
The EQM 32 receives condition input from the internal CTERM signal and external EQI signal. The EQM 32 can respond to a condition input on a selected one of these two condition inputs to execute an on line event qualified test monitor operation. The EQM receives external clock input from the CK1/2 output from MX1 40 in FIG. 2. The EQM 32 operates synchronous to CK1/2 input during execution of an on-line event qualified test monitor operation. The EQM 32 receives input from the EQM enable (EQENA) signal output from the command bus 44. When EQENA is set high, the EQM controller (internal to the EQM 32) is enabled to output the required control, in response to a condition input, to execute an event qualified test monitor operation in the TCR and/or memory buffer.

Detailed Description Text (47):
When a match is found between incoming data on the ODI inputs and the EXPDAT, the EQM 32 outputs a high logic level on the TGATE output. The TGATE output is routed to the TCR 28 and memory 30 to enable a test monitor operation. Also, when the TGATE output is high, the AND gate 66 in FIG. 7 is enabled to pass the CK1/2 clock input to the SYNCK signal. The SYNCK signal is routed to the TCR 28 and memory 30 to provide clocking for an on-line test monitor operation. In addition, the EQM 32 outputs the occurrence of a match condition on the external EQO output signal to inform neighboring devices of the

match. The EQO signal can be used to qualify a more global event qualified test operation using the external AND feedback network 24 shown in FIG. 1.

Detailed Description Text (68):
During on-line PSA or sample instructions, the mode 2 input signal will be set to allow the TGATE and SYNCK signals from the EQM 32 to be input to the test register via multiplexers 86 and 88. During this test mode, the TGATE signal will be set high to enable the SYNCK and to select the PSA/sample mode of operation in the test cells of the test register. The TGATE signal is set high in response to an input condition according to the type of protocol selected as shown in FIG. 7a, 7b, 7c, or 7d. If a PSA operation is being performed, the PSAENA input to the test register will be set high. If a sample operation is performed, the PSAENA is set low. The data appearing on the ODI0-15 inputs is clocked into the test register cells during each high clock pulse on the SYNCK input. After the PSA or sample operation is complete, the data or signature collected is shifted out for inspection via a TCR read instruction.

Detailed Description Text (87):
During the on-line PSA test instruction, the TCR 28 receives control from the internal EQM 32 via EQM control bus 52 to compress the data appearing on the ODI inputs into a 16 bit signature. After the data is compressed, the resulting signature can be shifted out of the TCR for inspection via a TCR read instruction.

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L7: Entry 8 of 31 File: USPT Oct 10, 2000

DOCUMENT-IDENTIFIER: US 6131171 A
TITLE: Process of testing and a process of making circuits

Brief Summary Text (5):
The ability to dynamically (i.e., during normal operation of the circuit board) observe the data passing between integrated circuits in real-time allows monitoring of the functional interactions between multiple integrated circuits on substrate, such as a circuit board. Such a test can reveal timing sensitive and/or intermittent failures that would otherwise not be detectable without the use of expensive testers and mechanical probing fixtures. The ability to dynamically observe system data buses in real-time facilitates system integration, environmental chamber testing, remote diagnostic testing, and built-in self testing.

Detailed Description Text (6):
In operation, the DBMs 20 and 22 are used to observe and test the digital signals carried on the buses 14-18 connected between the two integrated circuits 10 and 12. DBM devices operate in two modes: off-line test mode and on-line test mode. In the off-line mode, board circuitry is placed in a test mode and control for signal monitoring is input to the DBMs 20 and 22 from the external test bus interface. The external test bus interface includes four signals: TCK, TMS, TDI, and TDO. TCK and TMS are the test clock and test mode select signals, respectively, from the external test controller. TDI and TDO are the serial test data input and output signals used to connect DBMs and other devices conforming to the IEEE interface specification. Using the on-line mod, the board circuitry is functioning normally, and control for monitoring comes from the DBMs internal event qualification module (EQM) which is described in detail in connection with FIG. 7.

Detailed Description Text (10):
When the circuit of FIG. 1 is on-line and functioning normally, the first and second DBMs 20 and 22 can continue to monitor the data and address buses 14 and 16 using the internal EQM circuitry described below. During on-line monitoring the internal EQM of each DBM device 20 and 22 outputs control signals to capture the data appearing on the ODI inputs of the respective DBMs. The internal EQM operates synchronous to the control signal outputs from IC1 10 which are input to each DMB via the clock or CK inputs. To know when to capture data, the EQM circuitry within each DMB 20 and 22 has comparator logic which can match the data appearing on the ODI inputs against a known or certain expected data pattern or set of expected data patterns.

Detailed Description Text (47):
The EQM 32 receives condition input from the internal CTERM signal and external EQI signal. The EQM 32 can respond to a condition input on a selected one of these two condition inputs to execute an on line event qualified test monitor operation. The EQM receives external clock input from the CK1/2 output from MX1 40 in FIG. 2. The EQM 32 operates synchronous to CK1/2 input during execution of an on-line event qualified test monitor operation. The EQM 32 receives input from the EQM enable (EQENA) signal output from the command bus 44. When EQENA is set high, the EQM controller (internal to the EQM 32) is enabled to output the required control, in response to a condition input, to execute an event qualified test monitor operation in the TCR and/or memory buffer.

Detailed Description Text (49):
When a match is found between incoming data on the ODI inputs and the EXPDAT, the EQM 32 outputs a high logic level on the TGATE output. The TGATE output is routed to the TCR 28 and memory 30 to enable a test monitor operation. Also, when the TGATE output is high, the AND gate 66 in FIG. 7 is enabled to pass the CK1/2 clock input to the SYNCK signal. The SYNCK signal is routed to the TCR 28 and memory 30 to provide clocking for an on-line test monitor operation. In addition, the EQM 32 outputs the occurrence of a

match condition on the external EQO output signal to inform neighboring devices of the match. The EQO signal can be used to qualify a more global event qualified test operation using the external AND feedback network 24 shown in FIG. 1.

Detailed Description Text (71):
During on-line PSA or sample instructions, the mode 2 input signal will be set to allow the TGATE and SYNCK signals from the EQM 32 to be input to the test register via multiplexers 86 and 88. During this test mode, the TGATE signal will be set high to enable the SYNCK and to select the PSA/sample mode of operation in the test cells of the test register. The TGATE signal is set high in response to an input condition according to the type of protocol selected as shown in FIG. 7a, 7b, 7c, or 7d. If a PSA operation is being performed, the PSAENA input to the test register will be set high. If a sample operation is performed, the PSAENA is set low. The data appearing on the ODI0-15 inputs is clocked into the test register cells during each high clock pulse on the SYNCK input. After the PSA or sample operation is complete, the data or signature collected is shifted out for inspection via a TCR read instruction.

Detailed Description Text (90):
During the on-line PSA test instruction, the TCR 28 receives control from the internal EQM 32 via EQM control bus 52 to compress the data appearing on the ODI inputs into a 16 bit signature. After the data is compressed, the resulting signature can be shifted out of the TCR for inspection via a TCR read instruction.

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L5: Entry 1 of 2 File: USPT Aug 10, 1999

DOCUMENT-IDENTIFIER: US 5937154 A
TITLE: Manufacturing functional testing of computing devices using microprogram based functional tests applied via the devices own emulation debug port

Detailed Description Text (8):
As shown in FIG. 3, the computing device functional testing system 30 includes a test host computer 32 which interfaces to a computing system probe 34. A computing system probe as used hereinafter provides the ability to have run control of the computing device, and modify the contents of its memory, registers and I/O through an emulation debug port of the computing device. In the preferred embodiment communication is provided by use of a local area network (LAN) or a serial port. However, the method of communication is not limited to a LAN or serial port and any means of communication may be used to link the test host computer 32 and computing system probe 34. As previously mentioned, the computing device 36 is provided with an emulation debug port 38 for external access to the computing device's internal emulation debug hardware 37. The computing system probe 34 may be configured to control the emulation debug hardware 37 through the emulation debug port 38 of the computing device under test 36 via a hardware interface. The computing system probe 34 of the present invention provides the ability to have run control of the computing device, and modify the contents of memory, registers and I/O through the emulation debug port of the computing device. In the preferred embodiment, the computing system probe 34 also preferably provides debug emulation features including high-speed code downloading, target system programming of flash memory, and the capability of displaying as well as modifying the target computing device's memory and registers. For a computing device 36 which incorporates a Motorola 683xx family microcontroller, a Hewlett-Packard HP E3490A Processor Probe may be used to implement the computing system probe 34. The HP E3490A may be used via LAN to run the computing device 36 at full speed, download code, and set software and externally generated hardware breakpoints. For a computing device 36 which incorporates an Intel Pentium.RTM. processor, a Hewlett-Packard HP E3491A Pentium.RTM. Processor Probe may be used to implement the computing system probe 34. It is important to note that previously the computing system probe emulation technique was used as a low cost way to debug embedded software for processors which have on-chip debug features. It has not previously been utilized in a manufacturing test device. The computing system probe 34 connects to the debug port 38 of the computing device 36 and communicates with the computing device 36 to control internal emulation. The use of the computing system probe 34 allows the operation of system memory accesses and I/O device communication to be tested without using an external testing probe by controlling the debug features inside the computing device 36.

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L5: Entry 2 of 2 File: USPT Dec 31, 1996

DOCUMENT-IDENTIFIER: US 5590354 A
TITLE: Microcontroller provided with hardware for supporting debugging as based on boundary scan standard-type extensions

Detailed Description Text (2):
FIG. 1 shows a debugging environment with a microcontroller or microprocessor provided with the basic hardware for event tracing. Microcontroller 20 sits on target board 24 together with its system RAM memory 26. The microcontroller 20 is provided with a boundary scan or JTAG debug interface 46 that via JTAG board connector 28 and interconnection 34 is connected to host workstation 32 that itself has a JTAG interface card 30. The latter can interface to a plurality of JTAG interconnections such as 36. Microcontroller 20 has an on-chip system bus 48 that interconnects various subsystems, such as JTAG debug interface 46, a debug support unit 56 with an on-chip trace memory 58, processing element with caches 60, memory interface 62, and various further unnamed subsystems 50-54, such as an IO interface element. Via interconnection 64, debug support unit 56 is connected to a test probe or logic analyzer that has a serial-to-parallel converter 42, an event trace memory 40, and receives a time stamp from a source not shown. The event trace memory 40 via interconnection 36 that may be JTAG based is connected to host work station 32. System RAM 26 contains a debug section 44 that is addressed by a symbolically indicated debug trap vector. Finally, there is a direct interconnection 57 between the debug support unit 56 and JTAG interface 46.

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L8: Entry 1 of 21 File: USPT May 28, 2002

DOCUMENT-IDENTIFIER: US 6397354 B1
TITLE: Method and apparatus for providing external access to signals that are internal to an integrated circuit chip package

Brief Summary Text (6):
By way of background, U.S. Pat. No. 5,488,688, issued Jan. 30, 1996, to David R. Gonzales, et al., discloses a digital signal processor with a FIFO buffer configured on-chip to monitor a fixed set of internal bus signals. The FIFO buffer is coupled to a debug controller that is capable of operating in first and second modes. In the first mode, the CPU may be halted on the occurrence of one of four specifically-enumerated event conditions: after an external request; after a hardware breakpoint (occurrence of specific data or address values); after a software breakpoint (execution of a specific CPU instruction); or after a specified number of instructions have been executed. In the second mode, only the FIFO buffer is halted on the occurrence of an event condition. In either mode, the user may examine the contents of the FIFO buffer after a halt to determine what flow of software instructions were executed just prior to the event occurrence. An off-chip serial interface is used to communicate with the debug controller and to examine the contents of the FIFO buffer. The serial interface complies with the well-known Institute of Electrical and Electronics Engineers (IEEE) Standard 1149.1, "Test Access Port and Boundary Scan Architecture," also known as the Joint Test Action Group (JTAG) standard. A serial port conforming to this standard will hereinafter be referred to as a test access port or "TAP."

Brief Summary Text (7):
By way of further background, U.S. Pat. No. 5,473,754, issued Dec. 5, 1995 to Dale E. Folwell, et al., discloses a scheme for enabling an off-chip device to monitor the state of an on-chip 24-bit program counter in real time using an 8-bit port on the chip under test. Folwell assumes that discontinuities in the program counter will occur only in a limited number of situations. He then captures the contents of the program address bus only when one of these conditions occurs, and then sends those contents off chip via the 8-bit port. Because the contents of the program address bus are not captured with every increment of the counter, the volume of data that must be output via the 8-bit port is reduced.

Brief Summary Text (9):
By way of still further background, U.S. Pat. No. 4,910,417, issued Mar. 20, 1990 to Abbas El Gamal, et al., discloses an improved user-programmable interconnect architecture for logic arrays. Specifically, Gamal uses existing row-column selecting logic in combination with an output multiplexer for coupling user-selectable internal circuit nodes to a particular external chip pad for testing. Additionally, latches are provided for each chip input pin so that, with the assertion of an external signal, all chip inputs may be frozen. Then, the row-column select circuitry and output multiplexer may be used to probe nodes within the chip using the latched inputs as stimulus.

Brief Summary Text (12):
U.S. Pat. No. 5,867,644, issued Feb. 2, 1999, to Hunt et al., for instance, keeps the debug observation pads to a minimum by implementing on-chip multiplexers which are programmed through remote diagnose registers in order to statically multiplex groups of signals out to the observation pads. Signals that are in different sampling groups are then captured by reprogramming the multiplex select lines and rerunning the case. This approach provides significant reduction in the number of required observation pads and requires that the data capture instruments used, such as logic analyzers, run at the same speed as the device under test (DUT). It also assumes that the test case is repeatable across multiple runs.

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L8: Entry 14 of 21 File: USPT Feb 2, 1999

DOCUMENT-IDENTIFIER: US 5867644 A
TITLE: System and method for on-chip debug support and performance monitoring in a microprocessor

Brief Summary Text (6):
By way of background, U.S. Pat. No. 5,488,688, issued Jan. 30, 1996, to David R. Gonzales, et al., discloses a digital signal processor with a FIFO buffer configured on-chip to monitor a fixed set of internal bus signals. The FIFO buffer is coupled to a debug controller that is capable of operating in first and second modes. In the first mode, the CPU may be halted on the occurrence of one of four specifically-enumerated event conditions: after an external request; after a hardware breakpoint (occurrence of specific data or address values); after a software breakpoint (execution of a specific CPU instruction); or after a specified number of instructions have been executed. In the second mode, only the FIFO buffer is halted on the occurrence of an event condition. In either mode, the user may examine the contents of the FIFO buffer after a halt to determine what flow of software instructions were executed just prior to the event occurrence. An off-chip serial interface is used to communicate with the debug controller and to examine the contents of the FIFO buffer. The serial interface complies with the well-known Institute of Electrical and Electronics Engineers (IEEE) Standard 1149.1, "Test Access Port and Boundary Scan Architecture," also known as the Joint Test Action Group (JTAG) standard. A serial port conforming to this standard will hereinafter be referred to as a test access port or "TAP."

Brief Summary Text (8):
By way of still further background, U.S. Pat. No. 5,473,754, issued Dec. 5, 1995 to Dale E. Folwell, et al., discloses a scheme for enabling an off-chip device to monitor the state of an on-chip 24-bit program counter in real time using an 8-bit port on the chip under test. Folwell assumes that discontinuities in the program counter will occur only in a limited number of situations. He then captures the contents of the program address bus only when one of these conditions occurs, and then sends those contents off chip via the 8-bit port. Because the contents of the program address bus are not captured with every increment of the counter, the volume of data that must be output via the 8-bit port is reduced.

Brief Summary Text (10):
By way of still further background, U.S. Pat. No. 4,910,417, issued Mar. 20, 1990 to Abbas El Gamal, et al., discloses an improved user-programmable interconnect architecture for logic arrays. Specifically, Gamal uses existing row-column selecting logic in combination with an output multiplexer for coupling user-selectable internal circuit nodes to a particular external chip pad for testing. Additionally, latches are provided for each chip input pin so that, with the assertion of an external signal, all chip inputs may be frozen. Then, the row-column select circuitry and output multiplexer may be used to probe nodes within the chip using the latched inputs as stimulus.

Brief Summary Text (16):
In a still further embodiment, the output devices coupled to the state machine output bus include counters that are capable of keeping a tally of the number of times a certain user-defined event has occurred. The outputs from the counters may also be used as state machine inputs, so that one event may be defined as a function of a different event having occurred a certain number of times. The output devices also include circuitry for generating triggers that may be utilized both internal and external to the chip. The internal triggers may be used, for example, to halt the microprocessor clock, to latch the state of multiple test nodes (which may then be communicated off-chip via an external port for analysis), or to cause a trap within the microprocessor. The external triggers may be used, for example, to trigger similar diagnostic circuitry contained within neighboring chips, or to control external test

equipment. Moreover, user-configurable multiplexer circuitry is provided. This circuitry may be used to route a number of user-selectable signals from within the microprocessor to the chip's output pads, enabling them to be viewed externally for real-time analysis. This circuitry may also be used to select various internal signals to be used as state machine inputs.

Brief Summary Text (17):
In another embodiment, the invention includes a sophisticated method for debugging and monitoring the performance of a microprocessor. The method includes the steps of defining events by configuring the state machine just described to detect certain combinations of input signals, and also defining which actions should be taken in response to the detected events or sequences of events. Instructions are then executed on the microprocessor in real time until one or more of the events occurs.

Brief Summary Text (18):
In further embodiments, the method may include configuring on-chip comparators to generate match results based on signal patterns occurring on monitored nodes within the microprocessor. Both the steps of configuring the comparators and configuring the state machine may be accomplished by using the microprocessor's own instruction set to write control information to storage elements contained within the microprocessor. In addition, the method may include generating triggers that may be used to halt the microprocessor, trap the microprocessor, and/or latch the state of numerous test nodes within the microprocessor in "sample-on-the-fly fashion." If the latter aspect of the method is employed, further steps may include communicating the state of the latched test nodes to an off-chip device using a port built into the microprocessor. This aspect of the method enables viewing the microprocessor's state in "snapshot" fashion. The method may also include configuring an on-chip multiplexer circuitry to route a group of user-selectable internal signals to external chip pads. This aspect of the method enables viewing the microprocessor's state in "real-time" fashion.

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L4: Entry 75 of 96 File: USPT Jan 3, 1989

DOCUMENT-IDENTIFIER: US 4796259 A
TITLE: Guided probe system and method for at-speed PC board testing

Detailed Description Text (23):
The architecture described above is especially well suited to acquiring data in an at-speed testing environment. The start, stop and qualification and data signals are received in real time from the UUT. The versatility of the above structure allows the user to easily set up synchronization of measurements for the various measurement sets in testing a particular UUT. The user program can be configured to easily select any desired start event, stop event, sample clock, and various sample windows from the signals available from the field maintenance processor, the four BNC connectors on the front of the measurement module 12, and the four DSA bus conductors 13. The architecture ensures that all measurements taken with the same measurement module 12 setup will be correlated in time, so that the guided probe algorithm can use the time domain information supplied by the subsequently described variable time domain algorithm.

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L4: Entry 77 of 96 File: USPT Feb 9, 1988

DOCUMENT-IDENTIFIER: US 4724525 A
TITLE: Real-time data collection apparatus for use in multi-axis measuring machine

Detailed Description Text (8):
Turning now to FIG. 2, the real-time data collection computer 34 is shown in block diagram form. As in FIG. 1, X, Y, Z, A, and C data are input to real-time data collection computer 34 as indicated by box 36. Similarly, probe data is input to data collection computer 34 as indicated at box 35. The digital data from the X, Y, Z, A, and C axes are input to a counter 50. The digital data from probe 20 are input to a counter 52. Latch 54 is provided to simultaneously capture data from the X, Y, Z, A, and C axes together with data from the probe in response to a data capture, or latch signal. The captured data is held in registers 56 for subsequent processing. A data capture or latch operation is effected either by an internal clock which produces periodic data capture pulses, by a distance trigger signal which produces a data capture pulse when a machine axis or combination of axes has travelled a predefined distance increment, or by an external manually actuable switch. A measuring machine operator can effect data capture by actuating the manual switch.

Detailed Description Text (9):
The three modes of data capture are illustrated in FIG. 2 by a clock 60, a distance trigger switch 61, and an external switch 62 which are coupled to a latch mode switch 58. When the internal data capturing mode is in use, pulses from clock 60 will be connected to latch 54 via latch mode switch 58. When in the distance mode of data capture operation, a data capture signal produced by distance trigger switch 61 is coupled to latch 54 via latch mode switch 58. When in the external mode, a data capture signal produced by the manually actuable switch 62 is coupled to latch 54 via latch mode switch 58. The latching of data by real-time data collection computer 34 results, in effect, in a "snapshot" being taken of data from measuring machine 10 upon occurrence of a data capture signal. By simultaneously capturing data from the machine axis sensors and the machine probe, extreme accuracy is assured. At any given moment when data is captured, the machine operator can be confident that readings are taken from the X, Y, Z, C, and A axis at precisely the same moment that data are taken from the probe. This procedure affords an accuracy in measuring heretofore unobtainable in an automated measuring machine.

Detailed Description Text (13):
In an alternate embodiment set forth in FIG. 3, real-time data collection computer 34 can simultaneously capture data from the X, Y, Z, A, and C sensors (e.g., laser interferometers) and a multi-dimensional analog probe. As in FIG. 2, the X, Y, Z, A, and C data are input to data collection computer 34 as indicated by box 36. Similarly, probe data are input to data collection computer 34 as indicated at box 35. The mechanism for latching the X, Y, Z, A, and C data is the same in FIG. 3 as in FIG. 2. In capturing data from an analog probe, however, an analog to digital converter 88 must be provided. Since the analog to digital conversion does not occur instantaneously, a period of time must be provided for completion of the conversion prior to reading data from registers 56. Thus, analog to digital converter 88 (which may be built into an analog probe used with measuring machine 10) provides a data ready signal on line 92 for enabling read circuitry 90 to read data from registers 56 only after the analog to digital conversion has been completed and the converted data has been stored in registers 56. When an internal (clock) or external (manually actuated switch) pulse is provided to latch mode switch 58, analog to digital converter 88 immediately samples the data from the probe and commences analog to digital conversion. At the same instant, the X, Y, Z, A, and C data is captured and latched into registers 56. After the captured probe data is converted and stored in registers 56, a data ready signal is generated by converter 88 which enables circuitry 90 to read the data from registers 56. The data which is read is output on lines 94 and processed in the same manner

discussed above with respect to FIG. 2.